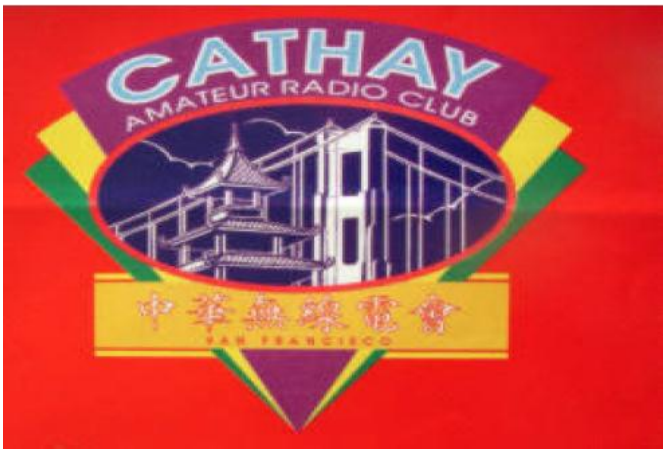

Cathay November 2013

www.cathayradio.org

President: George Chong, W6BUR **email:** *W6BUR@comcast.net*

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Vice President South: Bill Fong, *W6BBA* - **email:** w6bba@arrl.net

Secretary/Membership: Rodney Yee, *KJ6DZI* - **email:** rodyee2000@yahoo.com

Editor: Rodney Yee, *KJ6DZI* - **email:** rodyee2000@yahoo.com

Treasurer: Vince Chinn aka Mingie, *W6EE* - **email:** vince@vincechinncpa.com

Web Master: Edison Fong – *WB6IQN* - **email:** edison_fong@hotmail.com

Mission: The Cathay Amateur Radio Club is basically an active social club of Ham Radio Operators and their spouses. We support local community requests for HAM emergency communications. Several of us are trained in CPR/ First Aid and are involved with community disaster preparedness.

Monday Night Net Time: 9 PM Local Time/PST, Frequencies: 146.67MHz -600KHz PL85.4 and 442.70 +5MHz PL 173.8. The repeaters are linked only during the CARC Monday night net.

Update: Link to repeater 442.70 is currently not active until further notice.

The CARC Monday night net is the best way to find out the latest club news.
All check-ins are welcome.

Message from the President: George Chong, *W6BUR*

Hello CARC Members and Friends,

Can you believe that it is November already, where did this entire year go! Well, at least we have all the wonderful holiday parties to celebrate the remainder of the year.

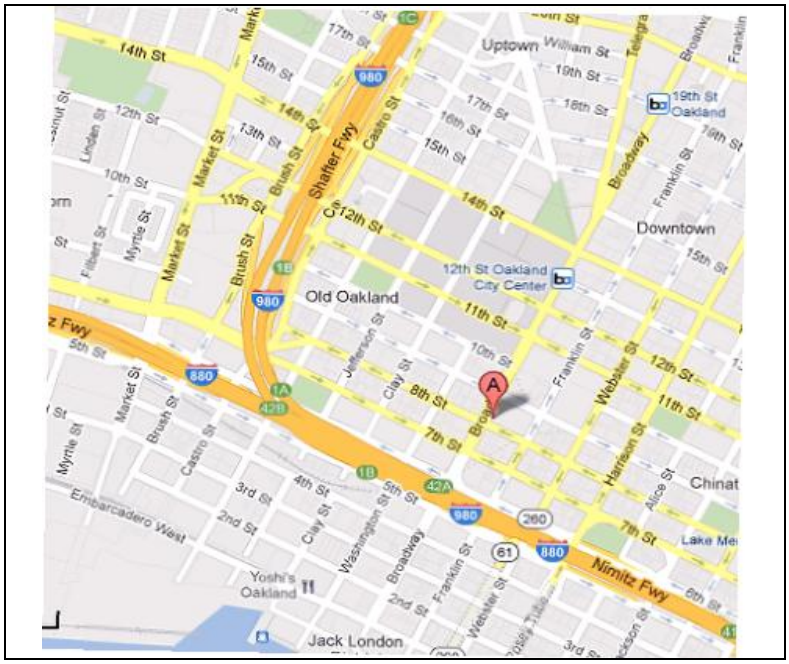
Veteran's Day Luncheon

Please join us for the CARC annual luncheon celebration of Veteran's Day, 11am on Monday November 11, 2013 at the restaurant below:

Buffet Fortuna
800 Broadway Street
Oakland, CA 94607
(510) 839-1688

The restaurant is an all you can eat American, Japanese and Chinese seafood buffet style food. The cost is $9.99 per person and for seniors it is $8.99. All soft drinks, coffee and tea are included with the price plus tipping is optional. The dinning time is limited to 2 hours, however have never seen it enforced for the luncheon period. Of course it does help a lot that CARC member Gilbert Gin, (KJ6HKD) is with going to be with us as he has considerable influence with the restaurant. I am usually stuffed to the gills within the first hour of eating the delicious food.

Map of the restaurant location is shown below:



U**pcoming Christmas Party**

On Saturday December 14, 2013 our esteemed CARC member Edison Fong (*WB6IQN)* will host a wonderful Christmas party at his home. The raffle prize will be dual band Baofeng radio with no tickets to buy. Every ham will be issued one ticket free. Please "Stay Tune" (yes, pun was intended for us radio folks) for the CARC December 2013 newsletter for more details.

Featured Tech Article

In the April 19, 1965 Electronics Magazine, Intel co-founder Gordon Moore's wrote an article that became known as Moore's law. Moore's law has been refined over time and the entire engineering community knows it as: "*The density of (silicon) transistors is doubling every 24 months".*

Moore's law was really a prediction/observation by Gordon Moore and that it would continue for the next ten years. Well it turns out that Moore's law has been uncannily held up for the subsequent 45 years and only slowed down in 2010 and seem to be on the verge of ending with the present 32 nanometer (billionth of a meter) technology.

To put that size in perspective, more than 4 million 32nm transistors could fit in the period at the end of this sentence. The current (2013) Intel Core i7 CPU is made up of 1.4 billion transistors as compared to the circ. 1989 Intel 80486 CPU transistor count of 1.18 million transistors using 1 micrometer (millionth of a meter) manufacturing technology. That is over a thousand fold increase in transistor density within 24 years.

The present silicon based transistors are rapidly reaching the upper physical limits of size reduction and thereby halting further increases in performance. The reduction in size of the silicon transistors over the last 45 years has fuel the increases in raw computing power and capacity of our computers, smart cellular phones, HAM radios, tablets, TVs and other electronic devices.

This month's feature tech article discusses a new break though that is on the horizon that will allow Moore's law to continue on for quite a while. So please enjoy reading this article.

(Editor's Note – As a young engineering student, I can still remember sitting in my UC Berkeley micro-processor class and the professor quoting Moore's law. My first thoughts were: IMPOSSIBLE! What was this guy drinking last night? Yeah, back then I thought I knew it all and of course I was way off the mark).

CARC Final Wrap:

Chat sub s'em to all you CARC members! - George W6BUR

Public Service Announcements

HAM CRAM / HAM Licensing

For upcoming HAM Licensing locations please refer to:
http://www.arrl.org/find-an-amateur-radio-license-exam-session

Bart Lee – K6VK

LATEST ON CALIFORNIA HISTORICAL RADIOO SOCIETY (CHRS) BUILDING PURCHASE

The following statement was read at Radio Day By The Bay and is the latest information we have at this time about California Historical Radio Society's (CHRS) future at 601 Ashby:

"As you know, we have been fundraising for the last year with the goal of purchasing this building and land for CHRS' permanent home. We were supposed to buy the building and land from the new owner of KVTO as it emerged from bankruptcy. But, KVTO has now been sold to a company who is not inclined to sell CHRS the building and land.

We can safely report that our license to occupy KRE will be honored to its completion until December 31st of this year. We are not being asked to leave anytime soon and there is a possibility that we may be asked to remain beyond that date.

So, as much as we love it here, a museum needs a permanent home. We have already started an active search. We realize that we may be leaving a historical place, but the reality is that we need a permanent place for the CHRS collection, Maxwell and SOWP archives and Radio Hall of Fame.

The fund raising momentum is still with us. All of the major donors to the KRE purchase fund have assured us that their pledges will remain in place to purchase a permanent new home for CHRS."

For additional information see: http://www.californiahistoricalradio.com/

Auxiliary Communications Service (ACS)

The Auxiliary Communications Service (ACS) was organized by the San Francisco Office of Emergency Services (OES) following the 1989 Loma Prieta Earthquake to support the communications needs of the City and County of San Francisco when responding to emergencies and special events.

The Auxiliary Communications Service holds General Meetings on the third Tuesday of each month at the San Francisco Emergency Operations Center, 1011 Turk Street (between Gough Street and Laguna Street), from 1900 hours to 2100 hours local time. All interested persons are welcome to attend.

The ACS Net begins at 1930 hours (7:30 p.m.) local time each Thursday evening, on the WA6GG repeater at 442.050 MHz, positive offset, tone 127.3 Hz. The purpose of this net is to practice Net Control skills, practice checking in with deployment status in a formal net, and to share information regarding upcoming ACS events. Guests are welcome to check in. ACS Members should perform Net Control duty on a regular basis. On the second Thursday of each month, the net will be conducted on the output frequency of the WA6GG repeater, 442.050 MHz no offset, tone 127.3 Hz, simplex.

For more information, please attend an ACS meeting or check in on a net, or call 415-558-2717.

Upcoming meetings: Tuesday 7pm, Nov 19, 2013
Tuesday 7pm, Dec 17, 2013
Tuesday 7pm, Jan 21, 2014

Gilbert Gin (KJ6HKD)

Free Disaster Preparedness Classes In Oakland:
http://www.oaklandnet.com/fire/core/index2.html

CORE is a free training program for individuals, neighborhood groups and community-based organizations in Oakland. The underlying premise is that a major disaster will overwhelm first responders, leaving many citizens on their own for the first 72 hours or longer after the emergency.

If you have questions about the recertification process, you may contact the CORE Coordinator at 510-238-6351 or core@oaklandnet.com.

Free Disaster Preparedness Classes In San Francisco – NERT Taught by San Francisco Fire Department

RSVP to sffdnert@sfgov.org or call 415-970-2024 to register.
Visit www.sfgov.org/sffdnert to learn more about the training, other locations, and register on line.

Upcoming Special NERT Events.

November

6th: NERT Coordinators and Leaders Meeting 6:30pm-8:30pm, SFFD DOT*
All NERTs welcome
Register: https://www.eventbrite.com/event/8485338877

13th: Understanding the Bay Area's Tsunami Risk, Preparedness Efforts, and Emergency Response, 6:30p-8:30p
Speakers: Cindy Pridmore, California Geological Survey & Kevin Miller- CA Office of Emergency Services, San Francisco County Fair Building, 9th Ave and Lincoln Way inside Golden Gate Park. FREE and open to the public!
Register: https://www.eventbrite.com/event/8938454157

December

7th: NERT Staging Area Drill. All NERT grads welcome, 8:30a-1:00p SFFD DOT*
This drill focuses on setting up and managing a neighborhood team staging area. Practice Incident Command System skills. Bring: NERT ID, helmet, vest, gloves, water, pencil and go-bag. Wear long pants, sturdy shoes and sunscreen. Dress for weather.
Register: https://www.eventbrite.com/event/8955434947

*** SFFD DOT is the Division of Training @ 19th Street/Folsom. (enter through yard on 19th and park along back wall) Division of Training classroom is in the 1-story building directly next to the Fire Station on the corner.**

San Francisco Police Department: Auxiliary Law Enforcement Response Team(ALERT)

The Auxiliary Law Enforcement Response Team (ALERT) is a citizen disaster preparedness program designed. The ALERT program is for volunteers 16 years of age or older, who live, work, or attend high school in San Francisco. Graduates of the San Francisco Police Activities League (P.A.L) Law Enforcement Cadet Academy are also eligible to join. ALERT volunteers will first complete the Fire Department's Neighborhood Emergency Response Team (NERT) (www.sfgov.org/sfnert) training and then graduate into an 8 hour Police Department course specifically designed for ALERT team members.

ALERT members will work closely with full-time and/or Reserve Police Officers in the event they are deployed after a disaster. The Basic ALERT volunteer will have no law enforcement powers other than those available to all citizens.

Upcoming ALERT Training

ALERT training class will be held at the San Francisco Police Academy, in the parking lot bungalow, from 8am-5pm (one hour lunch break). A new class is schedule as follows: Saturday, January 18th, 2014

IMPORTANT- All participants must complete the background interview process in order to be eligible to attend the ALERT training class.

Eligible ALERT participants may register for the January 18th, 2014 training class by contacting the ALERT Program Coordinator, Mark Hernandez, at sfpdalert@sfgov.org, or by telephone at 415-401-4615. To register by email send your request to sfpdalert@sfgov.org with your NAME and PHONE NUMBER.

ALERT Information Meeting:

An informational meeting will be held at the San Francisco Police Academy, located at 350 Amber Drive, Parking lot bungalows, at **7pm on Thursday December 5, 2013**.

All members of the public are welcome. Interested individuals will have their questions about the program answered at the meeting.

For more information on the San Francisco Police Department ALERT Program, email us at sfpdalert@sfgov.org, or call Sergeant Mark Hernandez (SFPD, Ret.), SFPD ALERT Program Coordinator, at (415) 401-4615.

For additional information on the web please refer to:
http://sf-police.org/index.aspx?page=4019

Featured Tech Article Section:

Tiny compound semiconductor transistor could challenge silicon's dominance

MIT researchers develop the smallest indium gallium arsenide transistor ever built.

Helen Knight, MIT News correspondent - December 10, 2012

http://web.mit.edu/newsoffice/2012/tiny-compound-semiconductor-transistor-could-challenge-silicons-dominance-1210.html

A cross-section transmission electron micrograph of the fabricated transistor. The central inverted V is the gate. The two molybdenum contacts on either side are the source and drain of the transistor. The channel is the indium gallium arsenide light color layer under the source, drain and gate.
Image courtesy of the researchers

Silicon's crown is under threat: The semiconductor's days as the king of microchips for computers and smart devices could be numbered, thanks to the development of the smallest transistor ever to be built from a rival material, indium gallium arsenide.

The compound transistor, built by a team in MIT's Microsystems Technology Laboratories, performs well despite being just 22 nanometers (billionths of a meter) in length. This makes it a promising candidate to eventually replace silicon in computing devices, says co-developer Jesús del Alamo, the Donner Professor of Science in MIT's Department of Electrical Engineering and Computer Science (EECS), who built the transistor with EECS graduate student Jianqian Lin and Dimitri Antoniadis, the Ray and Maria Stata Professor of Electrical Engineering.

To keep pace with our demand for ever-faster and smarter computing devices, the size of transistors is continually shrinking, allowing increasing numbers of them to be squeezed onto microchips. "The more transistors you can pack on a chip, the more powerful the chip is going to be, and the more functions the chip is going to perform," del Alamo says.

But as silicon transistors are reduced to the nanometer scale, the amount of current that can be produced by the devices is also shrinking, limiting their speed of operation. This has led to fears that Moore's Law — the prediction by Intel founder Gordon Moore that the number of transistors on microchips will double every two years — could be about to come to an end, del Alamo says.

To keep Moore's Law alive, researchers have for some time been investigating alternatives to silicon, which could potentially produce a larger current even when operating at these smaller scales. One such material is the compound indium gallium arsenide, which is already used in fiber-optic communication and radar technologies, and is known to have extremely good electrical properties, del Alamo says. But despite recent advances in treating the material to allow it to be formed into a transistor in a similar way to silicon, nobody has yet been able to produce devices small enough to be packed in ever-greater numbers into tomorrow's microchips.

Now del Alamo, Antoniadis and Lin have shown it is possible to build a nanometer-sized metal-oxide semiconductor field-effect transistor (MOSFET) — the type most commonly used in logic applications such as microprocessors — using the material. "We have shown that you can make extremely small indium gallium arsenide MOSFETs with excellent logic characteristics, which promises to take Moore's Law beyond the reach of silicon," del Alamo says.

Transistors consist of three electrodes: the gate, the source and the drain, with the gate controlling the flow of electrons between the other two. Since space in these tiny transistors is so tight, the three electrodes must be placed in extremely close proximity to each other, a level of precision that would be impossible for even sophisticated tools to achieve. Instead, the team allows the gate to "self-align" itself between the other two electrodes.

The researchers first grow a thin layer of the material using molecular beam epitaxy, a process widely used in the semiconductor industry in which evaporated atoms of indium, gallium and arsenic react with each other within a vacuum to form a single-crystal compound. The team then deposits a layer of molybdenum as the source and drain contact metal. They then “draw” an extremely fine pattern onto this substrate using a focused beam of electrons — another well-established fabrication technique known as electron beam lithography.

Unwanted areas of material are then etched away and the gate oxide is deposited onto the tiny gap. Finally, evaporated molybdenum is fired at the surface, where it forms the gate, tightly squeezed between the two other electrodes, del Alamo says. “Through a combination of etching and deposition we can get the gate nestled [between the electrodes] with tiny gaps around it,” he says.

Although many of the techniques applied by the team are already used in silicon fabrication, they have only rarely been used to make compound semiconductor transistors. This is partly because in applications such as fiber-optic communication, space is less of an issue. “But when you are talking about integrating billions of tiny transistors onto a chip, then we need to completely reformulate the fabrication technology of compound semiconductor transistors to look much more like that of silicon transistors,” del Alamo says.

The team presents its work this week at the International Electron Devices Meeting in San Francisco.

Their next step will be to work on further improving the electrical performance — and hence the speed — of the transistor by eliminating unwanted resistance within the device. Once they have achieved this, they will attempt to further shrink the device, with the ultimate aim of reducing the size of their transistor to below 10 nanometers in gate length.

Matthias Passlack, of Taiwanese semiconductor manufacturer TSMC, says del Alamo’s work has been a milestone in semiconductor research. “He and his team have experimentally proven that indium arsenide channels outperform silicon at small-device dimensions,” he says. “This pioneering work has stimulated and facilitated the development of CMOS-compatible, III-V-based-technology research and development worldwide.”

The research was funded by DARPA and the Semiconductor Research Corporation.